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**OFFICIAL****AMENDMENT TO THE CLAIMS**

i-14. (Cancelled)

15. (Currently amended) The semiconductor device in accordance with claim 12 16, comprising said dielectric film being formed between at least either a side surface or only a part of said bottom surface of said capacitor lower electrode part and said insulating film.

16. (Currently amended) The semiconductor device in accordance with claim 12, A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;  
an insulating film, having an upper surface, being formed on said major surface of  
said semiconductor substrate to extend from said memory cell region to said peripheral  
circuit region, wherein said insulating film includes an upper insulating film and lower  
insulating film being different in etching rate from each other;

a capacitor lower electrode assembly, including first and second lower electrodes  
being adjacent to each other through a part of said insulating film, being formed on said  
major surface of said semiconductor substrate to extend up to a vertical position  
substantially identical to that of said upper surface of said insulating film in said memory  
cell region;

first and second openings formed in the insulating film, and the first and the  
second lower electrodes formed within the first and second openings, respectively;

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said first and second lower electrodes each of a cylindrical shape having an interior region;

wherein respective sidewalls of the first and the second lower electrodes are formed to extend in a longitudinal direction with respect to the major surface of the semiconductor substrate, each sidewall having a cross-section in the longitudinal direction which is substantially linear; and

a capacitor upper electrode being formed on said capacitor lower electrode assembly through a dielectric film to extend onto said upper surface of said insulating film, said upper electrode being formed on the interior region of each of the first and second electrodes.

said capacitor lower electrode assembly including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface the semiconductor device further comprising granular crystals on a surface of said capacitor lower electrode.

17- 20. (Cancelled)

21. (Currently amended) The semiconductor device in accordance with claim 12  
16, wherein

said part of said insulating film having a width being smaller than the minimum working size formable by photolithography.

22-23. (Cancelled)

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24. (Previously added) The semiconductor device in accordance with claim 21, comprising:

said capacitor upper electrode being formed to extend toward said peripheral circuit region,

an upper interlayer isolation film being formed on said capacitor upper electrode and having a contact hole exposing a surface of said capacitor upper electrode, and a peripheral circuit element protection film being formed under said insulating film in a region located under said contact hole--

25. (Currently amended) A semiconductor device including a memory cell region and a peripheral circuit region, comprising:

a semiconductor substrate having a major surface;  
an insulating film, having an upper surface, being formed on said major surface of said semiconductor substrate to extend from said memory cell region to said peripheral circuit region, wherein said insulating film includes an upper insulating film and lower insulating film being different in etching rate from each other;

a capacitor lower electrode assembly, including first and second lower electrodes being adjacent to each other through a part of said insulating film, being formed on said major surface of said semiconductor substrate to extend up to a vertical position substantially identical to that of said upper surface of said insulating film in said memory cell region;

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first and second openings formed in the insulating film, and the first and the second lower electrodes formed within the first and second openings, respectively;  
said first and second lower electrodes each of a cylindrical shape having an interior region;

wherein respective sidewalls of the first and the second lower electrodes are formed to extend in a longitudinal direction with respect to the major surface of the semiconductor substrate; and

a capacitor upper electrode being formed on said capacitor lower electrode assembly through a dielectric film to extend onto said upper surface of said insulating film, said upper electrode being formed on the interior region of each of the first and second electrodes,

said capacitor lower electrode assembly including a capacitor lower electrode part upwardly extending in opposition to said capacitor upper electrode and having a top surface and a bottom surface. The semiconductor device in accordance with claim 12, wherein

a side surface of said capacitor lower electrode has a curved plane; and

a first width of the first and second lower electrodes at their upper ends is narrower than a second width in a central portion, in the height direction, of the first and second lower electrodes.